AMENDMENTS TO THE CLAIMS:

1-2. (Previously canceled)

3. (Currently amended) A method for manufacturing a semiconductor device comprising:

implanting n-type impurities within an NMOSFET forming region during a formation of channel regions and n-type source/drain regions;

implanting boron ions for forming a channel region to adjust threshold voltage within said NMOSFET forming region divided by an element dividing region;

implanting two different ions after said implantation of boron, comprising:

implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse short channel effect to form arsenic ion implanted regions thereby forming said source/drain regions within said NMOSFET forming region;

after said implanting said arsenic ions, using a same photoresist mask as a photoresist mask used in said implanting said arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted region; and

performing a heat treatment to activate the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions, said buffer regions comprising phosphorous ions and extending beyond said source/drain regions, thereby suppressing transient enhancement diffusion (TED) of a boron implanted region; and

forming an NMOSFET having the source/drain.

4. (Previously presented) The method as defined in claim 3, wherein n-type impurities are implanted in the NMOSFET region to form an n-type extension region before said implanting said two different ions.

5. (Previously presented) The method as defined in claim 3, wherein a dosage of the arsenic ion is determined to obtain electrical characteristics required for the NMOSFET and

an acceleration energy and a dosage of the phosphorous ion are determined such that an ion-implanted region of the phosphorous ion extends beyond a bottom surface of an ion-implanted region of the arsenic ion.

6. (Previously presented) The method as defined in claim 3, wherein the acceleration energy of the arsenic ion is not greater than 15keV, and the acceleration energy of the phosphorous ion is not greater than 15 keV and is lower than that of the arsenic ion.

7. (Previously presented) The method as defined in claim 3, wherein the dosage of the arsenic ion is between 2 x $10^{15}/cm^2$ and 1 x $10^{16}/cm^2$, and the dosage of the phosphorous ion is between 5 x $10^{14}/cm^2$ and 1 x $10^{15}/cm^2$.

8. (Currently amended) A method for manufacturing a semiconductor device comprising:

implanting arsenic ions in a semiconductor substrate at a first acceleration energy level to form an arsenic ion implanted region;

after said implanting said arsenic ions, using a same photoresist mask as a photoresist mask used in said implanting said arsenic ions, implanting phosphorous ions in said arsenic ion implanted region at a second acceleration energy level lower than said first acceleration energy level; and

performing a heat treatment to activate said arsenic ions and phosphorous ions to form an n-type source/drain main region comprising arsenic and phosphorous ions, and an n-type source/drain buffer region comprising phosphorous ions, said n-type source/drain buffer region extending beyond said n-type source/drain main region,

wherein said first acceleration energy is no greater than 15keV and said second acceleration energy is no greater than 10 keV.

9. (Previously presented) The method as defined in claim 8, wherein said device comprises an n-type metal oxide semiconductor field effect transistor (NMOSFET).

10. (Previously presented) The method as defined in claim 9, wherein said NMOSFET

comprises a gate electrode formed over a channel region, and wherein said n-type source/drain buffer region separates said n-type source/drain main region from said channel region.

11. (Previously presented) The method as defined in claim 10, wherein said substrate comprises monocrystalline silicon and said arsenic ion implanted region comprises an amorphous silicon region.

12. (Previously presented) The method as defined in claim 11, wherein a p-n junction formed at a first interface between said channel region and said buffer region is separated from a second interface between said amorphous silicon region and said monocrystalline silicon.

13. (Previously presented) The method as defined in claim 11, wherein point defects generated by said implanting phosphorous ions are absorbed by said amorphous silicon, such that diffusion of said phosphorous ions during said heat-treating is suppressed.

14. (Previously presented) The method as defined in claim 3, wherein said first acceleration energy level comprises about 10 keV or less.

15. (Previously presented) The method as defined in claim 8, wherein said first acceleration energy level comprises about 10 keV or less.

16. (Previously presented) The method as defined in claim 8, wherein said heat-treating comprises heat treating at about 1000°C for about 10 seconds.

17. (Previously presented) The method as defined in claim 8, where an arsenic concentration in said n-type source/drain main region is between $1 \times 10^{20}/cm^2$ and $5 \times 10^{21}/cm^2$ and a phosphorous concentration in said n-type source/drain buffer region is between $1 \times 10^{18}/cm^2$ and $5 \times 10^{19}/cm^2$.

18. (Previously presented) The method as defined in claim 3, wherein said boron ions are implanted in said semiconductor substrate to form a well region, said arsenic ions being implanted in said well region of said semiconductor substrate.

19. (Previously presented) The method as defined in claim 18, wherein said boron ions are implanted in said well region of said semiconductor substrate to form said channel region.

20. (Previously presented) The method as defined in claim 19, wherein said implanting boron ions to form said channel region comprises implanting boron ions at 30 keV at a dose of $1.0 \times 10^{13}/cm^2$.

21. (Previously presented) The method as defined in claim 20, further comprising:
forming a gate electrode on said channel region;
implanting arsenic ions in said well region to form extension regions;
performing a heat treatment to activate said arsenic ions in said well region; and
after said performing said heat treatment, forming sidewalls on said gate electrode.

22. (Currently amended) A method of manufacturing a semiconductor device, comprising:

forming extension regions by implanting first arsenic ions in a semiconductor substrate; and

forming source/drain regions and buffer regions extending beyond said source/drain regions, comprising:

implanting second arsenic ions in said semiconductor substrate at an acceleration energy level which is no greater than 15keV to form arsenic ion implanted regions adjacent to said extension regions;

<u>using a same photoresist mask as a photoresist mask used in said implanting said arsenic ions,</u> implanting phosphorous ions in said arsenic ion implanted regions at an acceleration energy level which is no greater than 10 keV for implanting said second arsenic ions, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted region; and

performing a heat treatment to activate said arsenic ions in said arsenic ion implanted regions and said phosphorous ions.

23. (New) The method as defined in claim 3, wherein said implanting said phosphorus ions is performed immediately after said implanting said arsenic ions without an intervening step.

24. (New) The method as defined in claim 3, wherein said phosphorus ions and said arsenic ions are implanted in a same surface.

25. (New) The method as defined in claim 3, wherein said buffer regions further comprise arsenic ions, an arsenic ion concentration in said buffer regions being greater than a phosphorus ion concentration in said buffer region.